Implementing Vocoder and HF Modem Algorithms Using the TMS320C31 DSP

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Abstract

This application report describes the implementation of a universal DSP module (UDM) to vocoders for a range of bit rates and to modems operating in the voice-band range. The UDM is based on the Texas Instruments (TI™) TMS320C31 DSP.

Difficulties in vocoder design are examined as well as measurement results for the HF modem under simulated HF channel environments. The error correction coding is varied among several methods during the HF modem measurement.

A functional description of the DSP module is included. The design described in this project enables the system to support vocoders with a bit rate range of 1.2 to 32 kb/s and HF modems with a bit rate range of 1.2 to 4.8 kb/s. An effective method of linear prediction parameter evaluation is presented for the bit rate range of 1.2 to 4.8 kb/s.

Parallel HF modem functionality and experimental research results on HF channel characteristics are also presented. The HF channel is simulated in real time using the PC-plugged DSP module. The fast synchronization approach is applied to a real world signal with a large frequency offset. Various methods of coding are compared.

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Introduction

Digital signal processors – effective means for realization of telecommunications devices in baseband frequency range. The most used among such devices - vocoders for speech compression and modems for digital data transmission over communications channels. General in realization of these devices is the presence of the analog-digital interface from one end and digital – with other. It lets to build both types of devices on the same hardware platform. At development of such platform it is necessary to take into account specific peculiarities of vocoders and modems in a part of tuning under clock frequencies of digital data receiving and transmitting.

In the section, *Universal DSP Module*, of the present article a functional scheme of the universal DSP module is described on the basis of which a number of vocoders in a rage of bit rates 1.2 and 32kbit/s and HF modem on bit rates of 1.2 and 4.8 kbit/s are realized.

In the section, *Vocoders*, some peculiarities of vocoders algorithms are stated. In particular for rates 1.2 to 4.8 kbit/s an effective method of linear prediction parameters evaluation is offered.

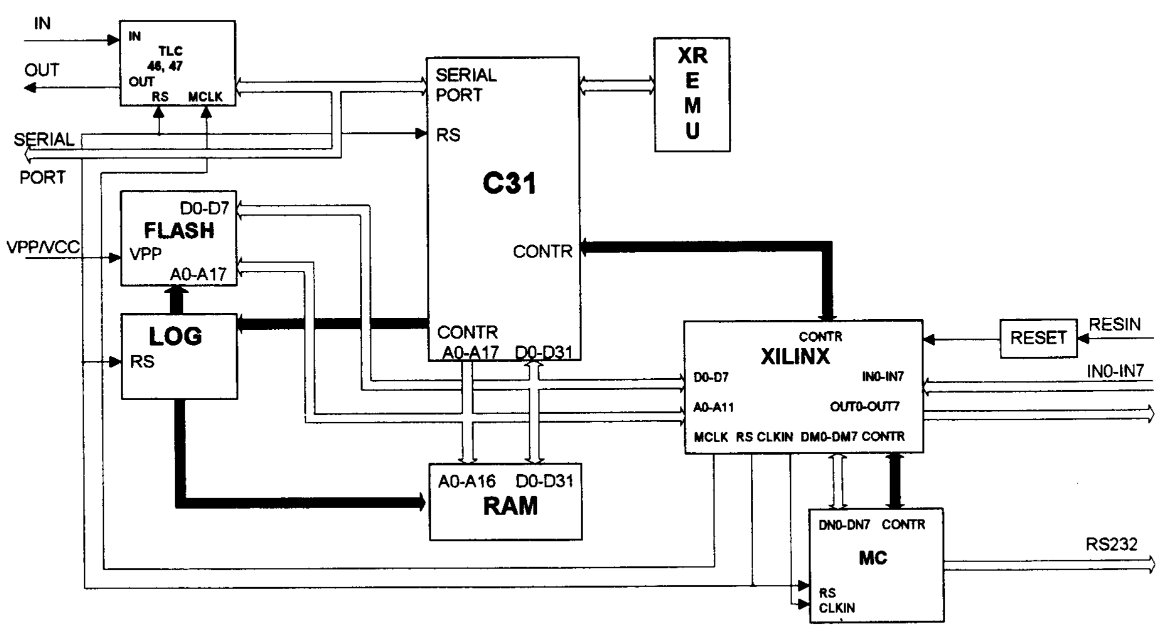
In the section, *High Frequency Modem*, bases of the parallel HF modem functioning and results of an experimental research of its characteristics over HF channel are stated. HF channel is simulated in real time using the PC-plugged DSP module. The fast synchronization approach is offered using the working signal in conditions of a large frequency offset. Various methods of coding are compared.

Universal DSP Module

The functional scheme of the module is submitted on Figure 1. It consists of

- TMS320C31PQL50 DSP with external 8-bit ROM (256K) and 32K or 128K of flash memory
- Analog/digital interface contained in the TLC3204X integrated circuit (IC)
- Control and interface logic block contained in the Xilinx's XC3030A FPGA IC
- Microcontroller (MC) TMS370C710
- Some standard interface logic ICs used for control signals for the DSP and memory

Figure 1. Functional Scheme



The process of module initialization can be shared into three stages:

- XC3030A initialization (configuration block is loaded from a flash memory over 8 bit data bus)
- Boot load of the program for the TMS320C31 DSP
- Initialization of the TLC3204X over the serial port of the DSP

The FPGA IC is intended for:

- Creates bi-directional 8 bit data bus between DSP and MC
- Creates 8 bit control channel (8 inputs and 8 outputs)
- Creates various control signals for the DSP and for the MC

The TMS370C710 MC lets to realize the interface RS-232 or any other interface for communication with external devices. Main DSP feature is an opportunity of independent control of ADC and DAC sampling frequencies. It is often necessary for realization momem PLL or tuning under colck frequencies, specifying a vocoder bit rate. Such opportunity is provided at the expense of digital *phase detector* (PD) design on base FPGA logic. Harmonic (subharmonic) frequencies of master clock TLC and clock frequencies determining receiving(transmitting) rates should be fed to the inputs of PD. Phase detector gives out logic 0 or 1. It depends on sign of deviation of these frequencies from each other.

This information is transmitted to DSP using one least significant bit (if it necessary to change a sampling frequency only ADC or DAC) or two least significant bits (if it necessary to change a sampling frequency as ADC and DAC) over 8-bit data bus between DSP and MC. The other 6 or 7 bits are used as information bits. The least significant bits are masked by DSP and used for control of sampling frequencies of ADC and DAC by loading of corresponding factors to the factors into the TLC3204X's control registers. Average sampling frequency will be followed to external frequency changes (for example to clock frequency, determining receiving of the digital information). For example there is 16 kHz clock frequency from external DCE (modem) in receiving mode of 16 kbit/s vocoder. This frequency is changed in result of the modem PLL working. Hence the DAC sampling frequency of a vocoder with nominal value 8 kHz also should be changed using above mentioned technique. There are two external sockets on DSP module: for DSP emulation and for loading of FPGA configuration file from PC.

Vocoders

A set of algorithms realized on the given hardware platform is chosen with a condition of universal character of application of the developed device. On one hand required universalness is determined by development of an algorithms and software supporting all accepted ITU recommendations for digital speech communications and speech compression: G.726, G.727, G.728. Realizations of two last newest recommendations G.723 and G.729 are now developed. And on other hand the most popular bit rates used in the various applications of telecommunications 1.2, 2.4, 4.8, 8, 16, 32 kb/s are supported by this board. For maintenance of speech coding in a range of bit rates from 8 kbps and below thee are used original algorithms and standards IS-54, USFS-1016, USFS-1015. We shall describe main peculiarities of realized algorithms.

Determination of the Spectral Parameter

At bit rates 1.2, 2.4, 4.8 kb/s the information about a current short-term spectrum envelope of a signal is transmitted with linear spectral frequencies (LSF),[1] which determined by roots of symmetric and anti-symmetric polynomials

$$P(z) = P_{p+1}(z) = A_p(z) + z^{-(p+1)} A_p(z^{-1})$$
$$Q(z) = Q_{p+1}(z) = A_p(z) + z^{-(p+1)} A_p(z^{-1})$$

for signal short-term spectrum pole model of a kind

$$H_p(z) = \frac{1}{A_p(z)} = \frac{1}{1 + \sum_{k=1}^{p} a_k z^{-k}}$$

where a_k = Linear prediction coefficients.

p = Order of model equal to 10 in considered algorithms.

Appropriate polynomials $P_k(z) = \sum_{i=0}^{k} P_{k,i} z^{-1}$ and

$Q_k(z) = \sum_{i=0}^{k} Q_{k,i} z^{-1}$ are determined for all intermediate models of a degree $k \le p$.

Split Levinson algorithm,[2] determining three-term recursive procedure of symmetric and anti-symmetric polynomials coefficients calculation,

$$P_{k+1}(z) = (1 + z^{-1})P_k(z) - \alpha_k z^{-1} P_{k-1}(z) \tag{1}$$

$$Q_{k=1}(z) = (1 + z^{-1})Q_k(z) - \beta_k z^{-1} Q_{k-1}(z) \tag{2}$$

plays fundamental role in calculations LSF. α_k and β_k are determined by Split Levinson algorithm.[2] At the initial conditions:

$$P_0(z) = 2, \quad P_1(z) = 1 + z^{-1} \tag{3}$$

$$Q_0(z) = 0, \quad Q_1(z) = 1 + z^{-1} \tag{4}$$

Further, we shall define scalar product for continuous complex functions φ and ψ in a kind.

$$(\varphi, \psi) = \sum \omega_i \varphi(\xi_i)\psi(\xi i_i)$$

Thus, each set $\xi_k \in C,\ k = 1, \ldots, n$ and positive numbers ω_k corresponds unique scalar product. Let now $\{\varphi_0, \ldots, \varphi_p\}$ is finite family of polynomials corresponding degree and $\varphi_o = 1$. For each above-stated scalar product it is possible to specify unique family of polynomials which is orthogonal in this scalar product and submitting three-term recurrence relation.[3]

$$\varphi_j(\xi) = (\xi - c_j)\varphi_{j-1}(\xi) - b_{j-1}^2 \varphi_{j-2}(\xi) \tag{5}$$

Each family in turn derivates a tridiagonal symmetric matrix

$$T = \begin{bmatrix} c_1 & b_1 & 0 & \cdots & \cdots & 0 \\ b_1 & c_2 & b_2 & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots & b_{n-1} \\ 0 & \cdots & \cdots & \cdots & b_{n-1} & c_n \end{bmatrix}$$

Thus this family is a family of characteristic polynomials for a matrix T[3],that is

$$\varphi_j(\xi) = \chi_j(\xi) = \det\left\lfloor \xi E_j - T_{i,j} \right\rfloor \tag{6}$$

where $T_{i,j}$ = Main sub-matrix of the order j. Moreover from the theorem Cauchy about sharing it follows that the polynomials sequence is a sequence of Sturm that is zeroes of the next polynomials alternate each other on the unit circle.[3]

The inverse is also true just if T is some tridiagonal matrix then it sets some sequence of polynomials being a sequence of Sturm and which in turn determines scalar product in which this sequence is orthogonal.[3]

We shall show now that polynomials submitting three-term recurrence of a kind (1) , (2) derives polynomials submitting three-term recurrence of a kind (5) . For this purpose we shall make the following replacement variable

$X = z + z^{-1} = 2\cos\omega$ at $z = e^{jw}$

Designate now through H_k (x) a function.

$$H_k(x) = \frac{Z^{k/2}}{1 + Z^{-1}} P_{k+1}(z) \tag{7}$$

Then it is easy to show that the functions which is determined by this way satisfies the following recurrence relation.

$$H_{k+1}(x) = (x + 2 - \alpha_{k+1} - \alpha_k) H_{k-1}(x) - \alpha_k \alpha_{k-1} H_{k-3}(x) \tag{8}$$

We now form new family of trigonometric polynomials from functions of even indexes.

$$\tilde{H}_k(x) = H_{2k}(x), \quad k = 0, \ldots, p/2 \tag{9}$$

In view of initial meanings (3) , (4) the family will be formed as follows:

$$\begin{aligned} &\tilde{H}_0(x) = 1 \\ &\tilde{H}_1(x) = x + 2 - 2\alpha_1 - \alpha_2 \\ &\tilde{H}_k(x) = (x + 2 - \alpha_{2k} - \alpha_{2k-1}) \tilde{H}_{k-1}(x) - \alpha_{2k-1}\alpha_{2k-2} H_{k-2}(x) \end{aligned} \tag{10}$$

Hence a tridiagonal matrix

$$T = \begin{bmatrix} 2\alpha_1 + \alpha_2 - 2 & \sqrt{\alpha_3\alpha_2} & \cdots & 0 & 0 \\ \sqrt{\alpha_3\alpha_2} & \alpha_3 + \alpha_4 - 2 & \cdots & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & \cdots & \cdots & \cdots & \sqrt{\alpha_{p-1}\alpha_{p-2}} \\ 0 & 0 & \cdots & \sqrt{\alpha_{p-1}\alpha_{p-2}} & \alpha_{p-1} + \alpha_p - 2 \end{bmatrix} \tag{11}$$

corresponds to this family of polynomials.

Thus agrees (6) the eigenvalues of the matrix are roots of polynomial $\tilde{H}_{p/2}(x) = H_p(x)$ and consequently polynomial $P_{p+1}(z)$ too. In an anti-symmetric case at replacement

$$F_k(x) = \frac{z^{k/2}}{1 - z^{-1}} Q_{k+1}(z) \qquad (12)$$

we shall receive tree-term recurrence

$$F_{k+1}(x) = (x + 2 - \beta_{k+1} - \beta_k)F_{k-1}(x) - \beta_k \beta_{k-1} F_{k-3}(x) \qquad (13)$$

To similar symmetric case we form family of polynomials

$$\tilde{F}_k(x) = F_{2k}(x), \quad k = 0,1, \dots, p/2$$

This family is set in view of initial values (4) by formulas

$$\begin{aligned} \tilde{F}_0(x) &= 1 \\ \tilde{F}_1(x) &= x + 2 - \beta_2 \\ \tilde{F}_k(x) &= (x + 2 - \beta_{2k} - \beta_{2k-1})\tilde{F}_{k-1}(x) - \beta_{2k-1}\beta_{2k-2}\tilde{F}_{k-2}(x) \end{aligned} \qquad (14)$$

Appropriate the tridiagonal matrix will have a kind

$$T' = \begin{bmatrix} \beta_2 - 2 & \sqrt{\beta_3\beta_2} & \cdots & \cdots & 0 \\ \sqrt{\beta_3\beta_2} & \beta_3 + \beta_4 - 2 & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \sqrt{\beta_{p-1}\beta_{p-2}} \\ 0 & \cdots & \cdots & \sqrt{\beta_{p-1}\beta_{p-2}} & \beta_{p-1} + \beta_p - 2 \end{bmatrix} \qquad (15)$$

An eigenvalues of a matrix T´ are roots of polynomial $\tilde{F}_{p/2}(x) = F_p(x)$ and consequently polynomial $Q_{p+1}(z)$ too. Thus, it has been shown that LSF are determined by eigenvalues of matrixes (11) and (15) . It should be noticed that as the consequence from the above-stated reasonings follows additional property of LSF alternateness for the next polynomials of a kind (10) or (14) .

In the practical relation as it is necessary to determine only quantizing values of LSF, their search can be organized with the bisection method or with the more effective secant method. However, in the given realization we used the tridiagonal QL algorithm.[3] The quantization of spectral frequencies is carried out on the basis of dynamic programming method.[4]

Peculiarities of Speech Coding Algorithms at 2.4 and 1.2 kb/s

Two original algorithms at these bit rates were developed. Classical model in a kind of pole filter excited by pulses and noise lays in a basis for the first. The format of transmitted bit stream in this case coincides the standard USFS-1015.[10] However, it is possible optionally to use improved algorithm of speech transmission in which the fifth state of a current signal frame describing voicing aperiodic frames of speech is entered. Two gains are transmitted instead of one into the bit stream of the fifth state.

Idea of MBE coder lay in a basis of the second algorithm.[11] As spectral parameters vector quantizing LSF and special transformed coded differences between a spectrum and 10th order pole model in pitch harmonics are transmitted in this case. Except these parameters the gain, pitch and five-band voicing information are transmitted. The synthesizer will form synthetic speech by mixing of appropriate amplitude pitch harmonics and output of the forming filter excited by noise. Speech transmission at 1.2 kbps bit rate is carried out with frame interpolation of the missed frames and application of described algorithms.

High Frequency Modem

The principles of modem design can be shared into two groups:

Parallel, in which the transfer of information occurs on several carriers and serial with one carrier. Advantages and the lacks of both principles were repeatedly discussed in the literature and it is difficult to prefer each of principles. Rather fast changes (fading) of the HF channel characteristics are occurred.

For serial modems complicative methods of adaptive filtering reduce the fading effect. The main condition of successful using of these methods is fast convergence of adaptation algorithms. It is necessary for correct work of filter in conditions of nonstationarity. Recent quantity of works devoted to this question has been much increased.[12]

For appreciable effects, significant computing resources are required. The parallel modems are more sready against fading in comparison with serial without complicative adaptive processing at the expense of presence of a guard interval and long-duration symbol interval.

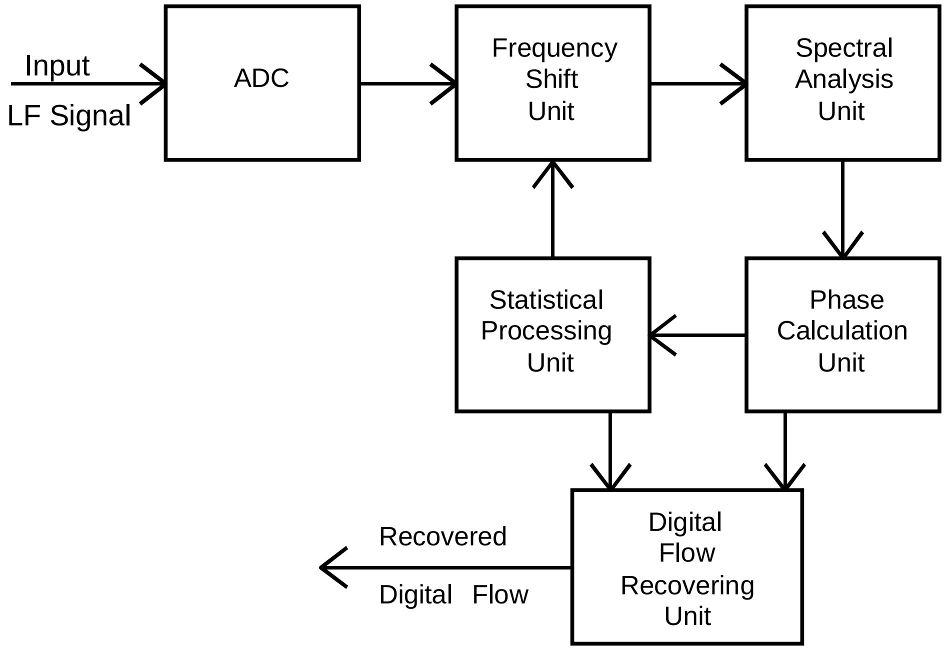
In the article parallel modem design is discussed. The structure is rather traditional. A sum of M harmonic carriers transfers LM bits using 2^L - ary DPSK modulation with frequencies $kf_0, (k = k_0 + 1, \text{where } l = 0, 1, ...(M - 1), k_0$ - initial number of a harmonic; f_0 - generating frequency; L - degree of modulation) in a frequency range 0.3+3.4 kHz on a symbol interval $T_{sym} = T_0 + \tau = \frac{N}{f_s}$ (where $T_0 = \frac{1}{f_0}$ interval orthogonality; τ - guard interval; f_s - sampling frequency).

So a bit rate of modem is LM/T_{sym} bits per second. The digital information, intended for transferred, is encoded by a error correcting coding. Then it feeds to the modulator. The discussion of methods of error correcting coding and decoding will be spent below.

The main problem of the demodulator is reliable receiving of the coded digital information in conditions of fading, significant frequency offset (±100 Hz), and additive noise of HF channel. Thus the symbol and carrier synchronizations should be carried out using only a working signal and in condition of minimal time of synchronization.

The generalized block diagram of the demodulator is resulted on a Figure 2.

Figure 2. Demodulator Block Diagram



Group baseband DPSK signal (low frequency signal) is fed to the input of ADC. The frequency shift unit implements frequency shift of group signal in correspondence to frequency offset. The value of a frequency offset is calculated by the statistical processing unit. At large allowable values of a frequency offset the procedure of carrier recovery will be carried out in three stages which will be explained below. In the spectral analysis unit a spectrum of a signal is calculated every P samples on carrier frequencies (frequency subchannels) using overlapped time windows with duration equalled $T_{0.}$ Thus spectrum is calculated N/P times per symbol interval. A phase spectrum of received signal is calculated by the phase calculation unit. Phases are found in every P samples and transferred to the statistical processing unit

The statistical processing unit solves the following problems:

- ❑ Carrier recovery that is reached by determination of a frequency offset, transmitted to the frequency offset unit
- ❑ Symbol recovery, reached by determination of a symbol interval edges

Both these problems are solved simultaneously by search of a minimum of the following functional:

$$E\left[\sum F\{\Delta_m \varphi(n, \Delta f)\}\right] \qquad (16)$$

where $\Delta_m \varphi(n, \Delta f)$ = deviation of a phase difference in the neighboring symbol intervals from the nearest permitted value 0, $\frac{\pi}{2^{L-1}}, 2\frac{\pi}{2^{L-1}}, ..., (2^L - 1)\frac{\pi}{2^{L-1}}$ in m^{th} frequency sub-channel and n^{th} time window at a Δf frequency offset of a group signal ; F{ } - square-law function; E operation of time average.

The functional minimization is carried out as over a frequency offset and over a clock interval during a symbol interval. The value of *m* in (16) can be equal to M or less. It is up to DSP computing resources and stage of carrier recovery.

At the first stage the rough tuning is occurred with the resolution of a PLL capture band of fine tuning, equalled $\Delta f_{cap} = \frac{1}{(2^{L+1} T_{sym})}$.

Thus divisible to a capture band Δf is chosen, ensuring a minimum (16) .

At the second stage, fine-tuning is made by definition Δf, at which the value of $E\left[\sum F\left\{\Delta_m \varphi(n, \Delta f)\right\}\right]$ is close to zero. It is supported by feedback loop from statistical processing unit to frequency shift unit.

And at last, at the third stage, minimization of (16) is made accurate to the frequency sub-channel. It is necessary when the value of frequency offset is more than f_0. In this case, calculation of (16) is made using *m* corresponding to the part of subchannels on edges of a working frequency range.

The described above procedure of synchronization reliably works in conditions of deep fading and significant noise. The heaviest computing expenses arise at the first stage of synchronization, especially if to carry out rough tuning for all possible Δf simultaneously to reduce the time of synchronization.

With this purpose fast recurrent algorithms of the spectral analysis were developed on the basis of Goertzel algorithm with decimation and Fast Fourier Transform (FFT). The functional minimization is made by simultaneous calculations (16) for all possible $r\Delta f_{cap}$, where r = 0, 1, $\frac{f_0}{\Delta f_{cap}} - 1$.

Further fine tuning and the tuning accurate to the frequency sub-channel (kf_0) is carried out in condition of $\Delta f = r_0 \Delta f_{cap}$, where r_0 ensures a minimum of (16).

It is necessary to notice that the minimization of functional (16) can be replaced by determination of its centre of gravity with some weight function. It allows to decrease an error probability.

Methods of error correcting coding used in the modem strongly influence to modem performance. In the described modem, various methods of coding were applied to improve the reliability of reception in conditions of fading:

- Diversity reception
- Reed-Solomon coding
- Convolution coding with various constraint lengths
- Trellis coding

Criterias for use of these methods were efficiency in conditions of fading and limited complexity of realization (1 TMS320C31 DSP). All measurements of an error probability were made in real time with use of HF channel model and realized on PC plugged board also based on the TMS320C31 and TLC3204X.

According to the CCIR recommendations (report 549),[13] two types of HF channel were considered: with average (2 rays, frequency spread = 0.5 Hz, delay between rays = 1 ms) and bad channel (2 rays, frequency spread = 2 Hz, delay between rays = 3 ms) conditions.

Moreover frequency offset and additive Gaussian noise were simulated. The resulted below curves of errors probability are received by measurement of an error probability for average and bad conditions (see Figure 3 and Figure 4). Each point of curve is received at transmission sample of 10 millions bit.

Figure 3. Modem Performance Under Average Conditions

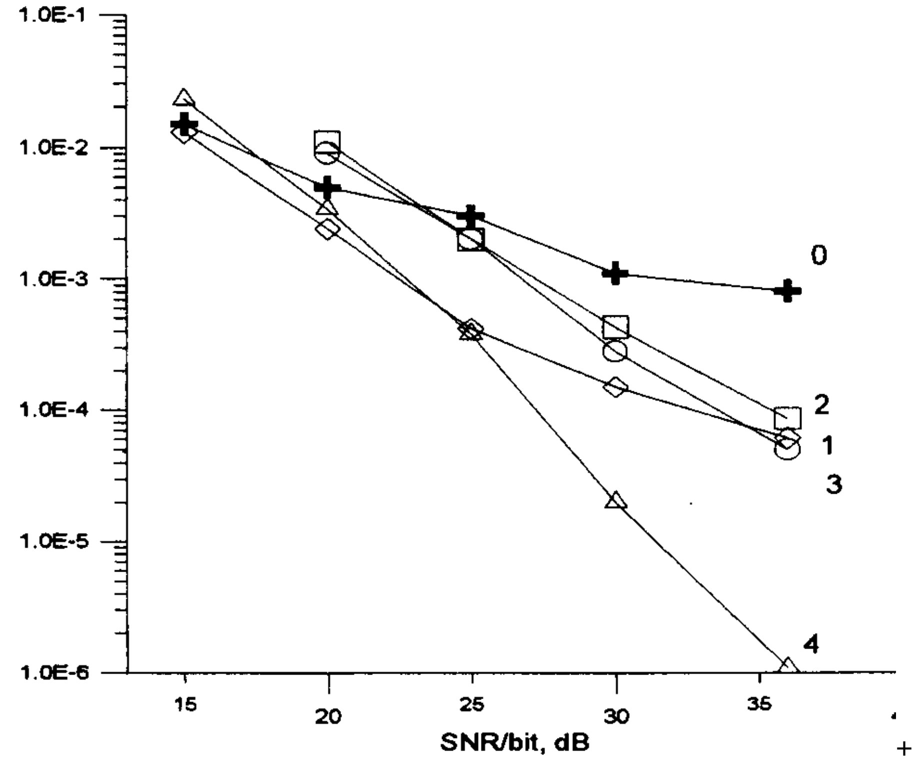
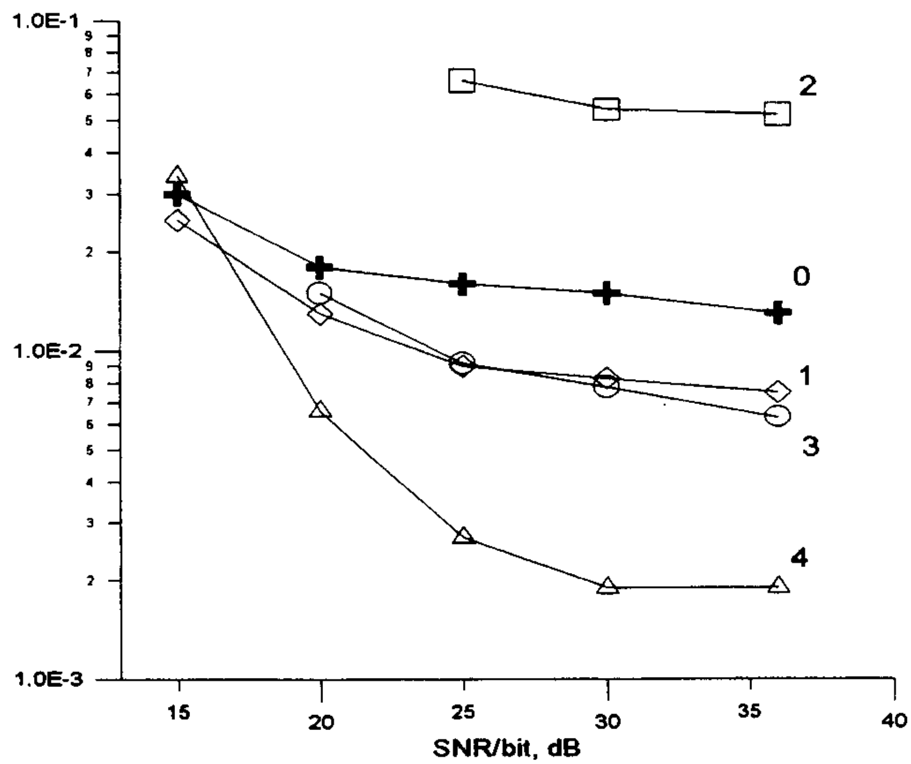


Figure 4. Modem Performance Under Bad Conditions



According to the technical requirements of the described modem, the allowable frequency range is (0.5÷3.0 kHz). It is a little bit narrowed in comparison with a standard voice-band range. Hence, at f_0 =50 Hz the maximum number of subchannels M is equal 47 if allowable frequency offset of (±100 Hz). The number of information bits over the symbol interval is equal to 60 at a bit rate of 2400 bit/s. For the HF channel, L should not be more than 3 because of hard propagation conditions. Thus, the maximum redundancy is close to 2, which can be received in view of the above-stated restrictions.

The various variants of coding were compared among themselves and with uncoded variant with the signal construction (M = 30, L = 2) over HF channel models under above mentioned average and bad conditions. Diversity reception had shown the worse performance than the reception with error correcting coding. So we present measurement results of the last one.

Following variants of coding were investigated:

- Reed-Solomon Code
- Convolution coding
- Trellis coding

A brief description of each coding method follows.

Reed-Solomon Code

The input information was coded by a Reed-Solomon code (12, 8) received by truncation from a code (15, 11) over a Galois field GF (16), with a generating polynomial

$$g(x) = x^4 + \alpha^{13} + x^3 + \alpha^6 + x^2 + \alpha^3 + x + \alpha^{10}$$

where α = primitive element of a field.

Input frame of 60 bits was divided by words of length 30 bits which were two zero's complemented up to 32 bits. Each word is represented in 48 bits after coding. Then two added zero bits were extracted coded words to create two 46 bit words which are fed to the modulator. Thus the coding was made on a grid of frequencies using the signal construction (M = 46, L = 2).

Convolution Coding

The structure of coding was corresponded to structure from references[14] with the number of cyclically multiplexed coders.

2/3-convolution coder was realized. Its constraint length V is equal to 6 and matrix of generating polynomials is:

$$\begin{bmatrix} x^3 + x^2 + 1 & x^2 + x & x^3 + x^2 + 1 \\ x^2 + x & x^3 + x^2 + 1 & x^3 + x^2 + x + 1 \end{bmatrix}$$

And two coder variants were tested for signal constructions (M = 30, L = 3) and (M = 45, L = 2).

Trellis Coding

Trellis coding[15] was developed with v = 4 on the basis of a signal construction (M = 30, L = 3). The structure of coding also corresponds the structure from reference[14] with the metric for fading channels.

Figure 3 and Figure 4 demonstrate modem performance for various variants of coding under following conditions: average conditions (Figure 3), and bad conditions (Figure 4).

- Curves with an index of 0 correspond to the uncoded variant.
- Curves with an index of 1 correspond to the Reed-Solomon code.
- Curves with an index of 2 correspond to convolution coding with a constraint length of v = 6 and signal constructions of (M = 30, L = 3).
- Curves with an index of 3 correspond to trellis-coding.
- Curves with an index of 4 correspond to convolution coding with a constraint length of v = 6 and signal constructions of (M = 45, L=2).

It is visible that even such simple code as a Reed-Solomon code gives appreciable improvement of the modem performance. Use of a convolution code with a signal construction of (M = 30, L = 3) can give even deterioration of the modem performance (see Figure 4).

It should be emphasized that use of a more simple Trellis-code (v = 4) with the special metric lets to achieve results not worse than by use of convolution code with V = 6 and Hamming metric. Presently we try to use more complex Trellis-coding. Nevertheless convolution code with a constraint length of v =6 and L = 2 (4PSK) shows the minimal error probability among realized variants. It is necessary to note that reliability of synchronization for L = 3 (8 PSK) is worse than at L = 2 (4PSK).

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