DSP UNITS FOR IP-TELEPHONY SYSTEMS

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Abstract. Two DSP units designed for usage in multichannel IP-telephony (VoIP) gateways are considered in this paper. DSP units are implemented in the form of PCI/ISA boards on the basis of TI's TMS320C54x family DSPs.

1. Introduction

In last years intensive investigations and development in the IP-telephony area are held. IP-telephony means real-time speech information transmission in packet-switched networks on the basis of IP-protocol (VoIP). IP-telephony gateways are used for connection PSTN and digital networks. These gateways implement all necessary conversions of speech and signaling information. Two DSP units were designed for usage in 2- and 16-channel IP-telephony gateways. In addition to DSP units these gateways [1] contain host PC running under Windows NT ™ and (in case of 16-channel unit) two analog interfaces boards with 8 PSTN lines per each. DSP units are implemented in the form of PCI/ISA boards on the basis of TI's TMS320C54x family DSPs.

2. Hardware Implementation

16-channel DSP unit. 16-channel unit is implemented in the form of PCI board and has 9 TMS320C54x DSPs. The block diagram of the device is shown on fig. 1. Interface part provides information input/output through external interfaces and controls all functional modules of the device. Computing part receives information from the interface part, processes it and transmits the results backward.

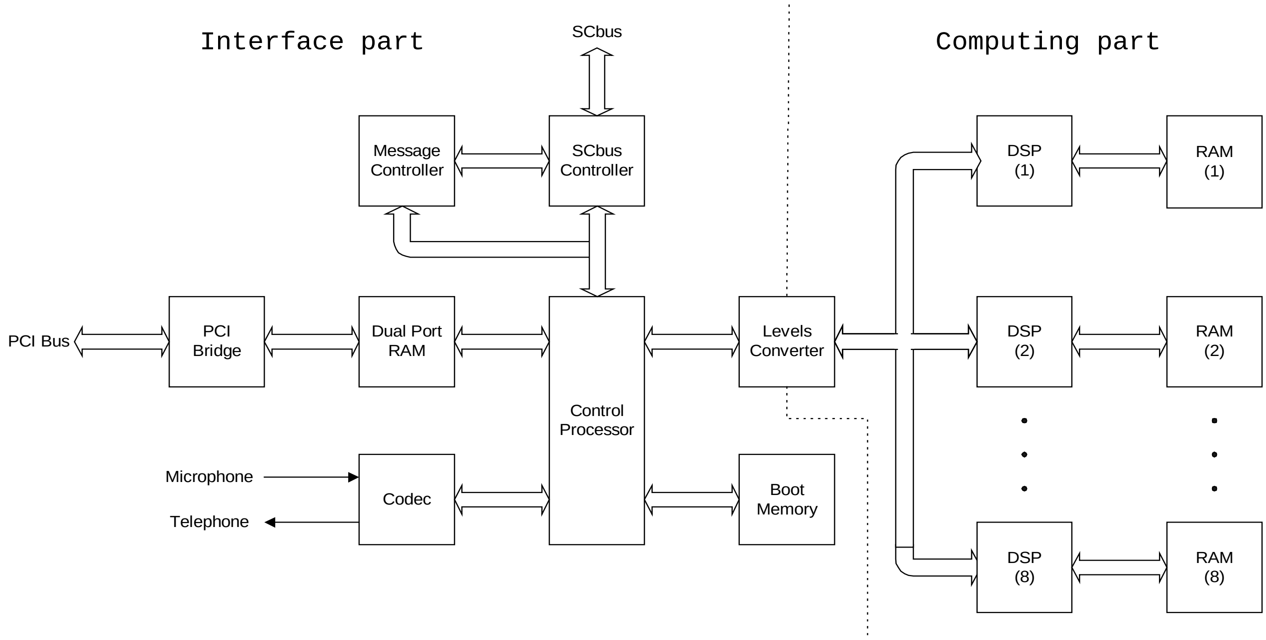

Fig. 1.

Control processor TMS320C542 (40 MIPS) which operates the whole board is the central node of interface part. It provides information exchange between 8 DSPs and PC via PCI-bus, speech signals transmission from the board of analog interfaces via SC-bus, and local handset usage. Communication with PC is implemented via Dual Port RAM, which is available for reading and writing both from PC (4K x 32) and from Control Processor (8K x 16). PCI-bus is connected with Dual Port RAM via PCI Bridge PCI9050 (PLX

Technology), which transforms PCI signals into local bus signals providing Dual Port RAM control. Control Processor is connected with SC-bus Controller SC2000 (VLSI Technology) and Message Controller SAB82526 (Siemens), which provide SC-bus usage. SC-bus controller directly operates the bus, which is used for speech data and control signals transmitting. Message Controller provides service communication channel implementation on SC-bus. SC-bus signals are taken out on a special connector to connect several analog interfaces boards. While working with handset, analogue and digital signals transforming is performed by module Codec, implemented on TCM320AC37 (Texas Instruments) chip. While Control Processor bootloading FLASH memory (M27C512 chip) is used. Computing part programs loading into 8 DSPs is maintained from PC. Levels Converter serves for coordination of voltage and buffering levels of Interface and Computing parts.

Computing part consists of 8 similar nodes, each containing TMS320LC548 (80 MIPS) DSP and external RAM (64K x 16). To simplify the figure 1 only three nodes (1, 2 and 8) are shown. Information exchange is performed via Host Port Interface. Signals are buffered in Levels Converter module.

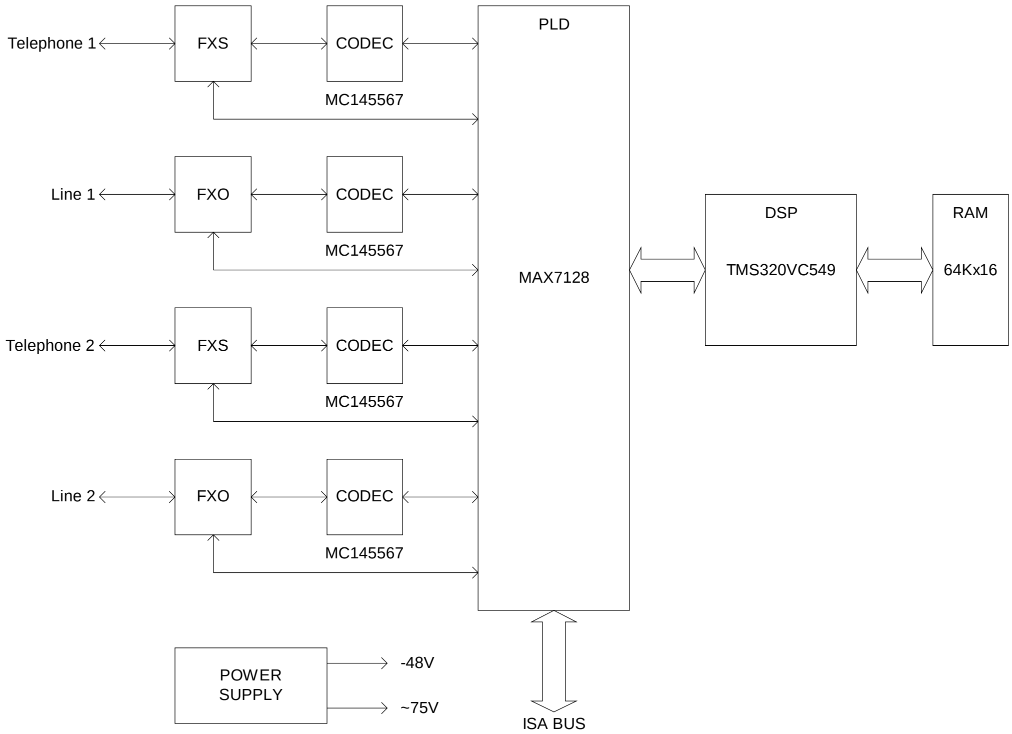

Fig. 2.

Compact 2-channel DSP unit. This unit is implemented in the form of ISA board and contains built-in analog interfaces. The block diagram of the device is shown on fig. 2. There are two interfaces on the board: FXS – to connect telephone sets (Telephone 1 and Telephone 2) and two interfaces FXO – to connect telephone lines (Line 1 and Line 2). MC145567 (Motorola) codecs are used in each channel as ADC/DAC. Board control and signals processing are performed by TMS320VC549 DSP (100 MIPS). External RAM (64K x 16) is connected to the DSP. Schemas of DSP and FXS/FXO connection, and information exchange with PC via ISA-bus are implemented by PLD MAX7128 (Altera) chip. Power Supply module provides 48 V (DC) for lines supply and ~75 V (AC) for ring tone. Current analog interface selection is made by software.

3. Functional Implementation Features.

Functional scheme of signal processing in DSP unit of IP-telephone gateway is presented on fig.3 (only one channel shown). Analog signal from telephone line or from telephone set is passed through hybrid circuit, ADC, and converted to 64 kbps bit stream using A-law (ITU-T Recommendation G.711). Then this bit stream comes to DSP unit.

Echo canceller complies the requirements of ITU-T G.165 Recommendation, but two new elements appear. Adaptive threshold in double talk detection allows suppressing of echo signals greater than –6 dB. Echo canceller's convergence speed control based on speech parameters analysis allows to reduce adaptation speed on narrow-band signals, for example, telephone service signals and voiced speech frames.

Then the signal passes through the Automatic Gain Control (AGC) unit and comes to the Speech Encoding block. The following speech encoding algorithms are implemented: proprietary CELP-coder operating at 4.6 kbps (main features of the algorithm: enhanced lost packages interpolation mechanism – speech intelligibility is saved up to 15% of single losses; quick search through algebraic codebook) [2]; CS-ACELP speech coder operating at 8 kbps (ITU-T G.729 Recommendation Annexes A and B); MP-MLQ/ACELP coder (ITU-T G.723.1 Recommendation Annex A) operating at 6.3 and 5.3 kbps. Voice Activity Detector (VAD) is included in all vocoders. During pauses it reduces output bit stream nearly to zero. Implementations of G.723.1 (Annex A) and G.729 (Annexes A and B) were tested against correspondent testvectors.

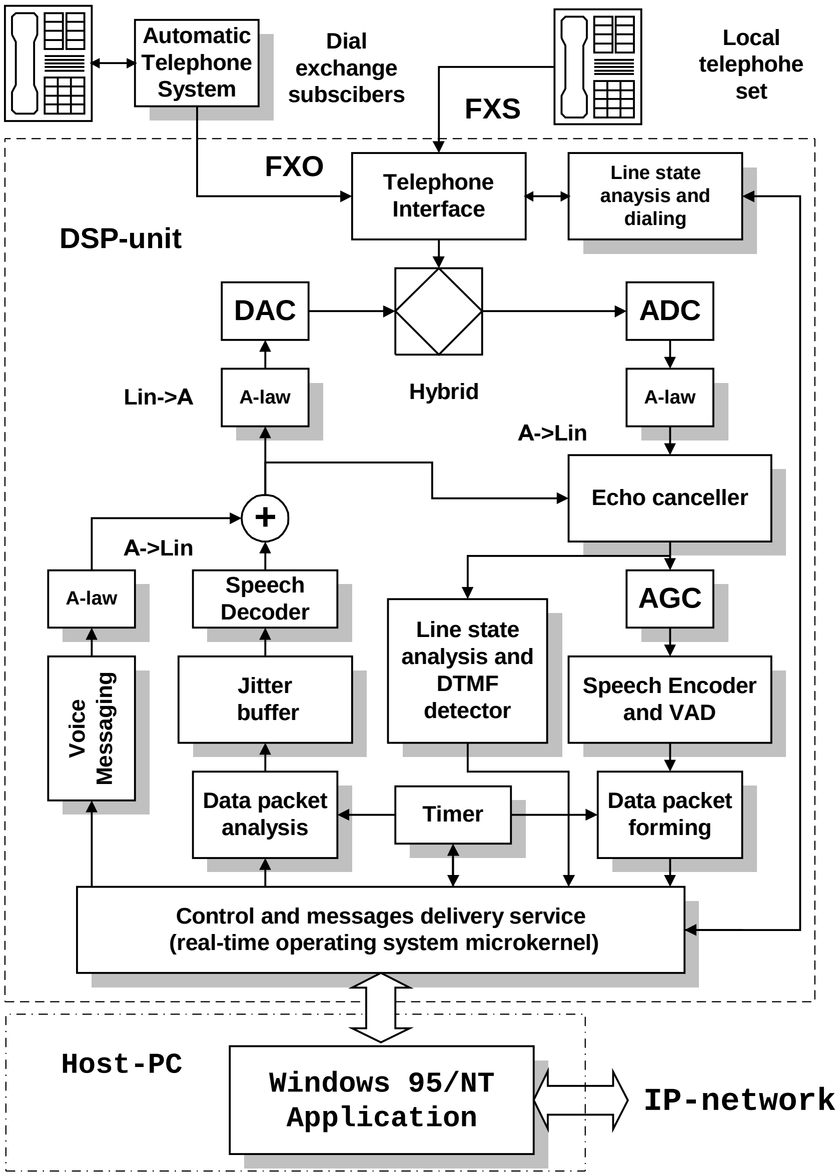

Fig. 3

Parallel to signal compression incoming signals analysis takes place. Following service signals are detected: “dial tone”, “ringing tone”, “busy/congestion” and DTMF. DTMF detector works with signals rate from 0 to –25 dBm and is stable to speech signals presence.

Then speech signal packets containing time marker and speech frame type are formed. These packets are sent to PC application and then to IP-network via UDP protocol.

On the receiving side adaptive buffering of received packages to smooth network delivery time irregularities, packets sorting by time of synthesis, and missed packages interpretation as silence or lost frames are performed. Then speech decoding with lost frames interpolation, followed by digital-analog conversion, takes place. After that decoded speech signal is sent through the telephone line to subscriber. The decoder is automatically tuned to the incoming packet type, which allow switching vocoder’s type without connection break. The gateway sends to the subscriber voice messages, which come from PC and are set into outgoing speech flow.

4. Internal System Kernel Implementation Features

DSP unit's software is build on the base of embedded real-time operating system microkernel (uRTOS) containing unified input/output routines. This provides effective tasks processing, independent module's design, and whole system openness for upgrade and hardware configuration change. The system kernel solves following tasks:

- Providing input/output functions software interface for all control and signal processing modules and supporting them on hardware-level;
- Modules call according to their priorities in scenario;
- Processor's interrupts handling;
- Multichannel mode support.

Built-in uRTOS supports data exchange in the form of messages. This allows to unify interaction between functional blocks in distributed system, and to provide simple tools of data and command set expansion. Every routine can send and receive messages, and the system delivers them. The message consists of header with destination and source addresses, message code and length, and attached data packet. Messages' sending is carried out by system functions calls. The message is put in system output queue and depending on destination address is sent to function inside the DSP unit, to PC application, or to remote gateway via IP-network. All this is done transparent to sender function. Received messages are buffered by the system in input queue and are given to receiver function while its call occurs.

Besides message transmission, routines control and scenario of their calls inside DSP unit are performed by the system of semaphores, consisting of global flags set, accessible from any function by name.

Function call is performed according to scenario of two subscribers connection establishing, maintenance, and disconnection. System synchronization is defined by new speech frame availability. There are several priority levels. Real-time signal processing routines (A-law companding, echo cancelling, AGC, line state analysis, speech coding) are executed in the first turn, and are interrupted only in case of hardware interrupts occurring. Incoming queues and messages sorting form the second sort of routines. These tasks are carried out in background mode, returning control back to the system when new speech frame arrives. Besides that, the system supports delayed function call, which consists of automatic call of specified routine with control parameters transmission fixed amount of time later the target setting. This allows to take into account control message transmission delays and to introduce suitable timeouts system. Message input from PC by the user and debug information output on display or to the file are implemented by DSP unit and PC application for convenient debugging.

To simplify modifications and to provide software portability all logical part of the real-time operating system kernel is written on C language. To provide high performance all system input/output functions and interrupt handling routines are written on TMS320C54x assembly language.

5. Multichannelling

The processing of two channels in one DSP is performed independently on their states. Each channel has its own set of global flags, input and output message queues. Data processing routines calls are performed by the system sequentially within the speech frame (30 ms). In detail multichannelling implementation is discussed in [3]. In this case we chose external data memory pages switching method with common program code.

6. Vocoders Implementation and Debugging Features

The main feature of vocoders implementation is multichannelling – the ability to process several duplex channels on one DSP. In detail this question was investigated in [3]. It was shown there that the best way to provide multichannelling taking into consideration memory and processor's loading economy is channel descriptors switching. Data contexts of different channels are stored in different arrays, and the table of pointers is copied before current channel codec call (fig. 4).

For efficient implementation of algorithms nearly all code was written on TMS320C54x assembly language. Unfortunately, productivity of TMS320C54x C-compiler is rather poor, especially in comparison with TMS320C6xx C-compiler. But Code Composer™ provides brilliant opportunities in assembly code debugging, for example, file input/output, profiling, graphs, etc.

In contrast to ITU-T G.723/G.729 standards implementation, designing of proprietary vocoder needs test vectors selection. We select them on the stage of development and verification of fixed-point C-model, which was implemented using standard basic operators for computation in fixed-point domain. Both standard speech files and signals recorded with overloads (for examples, with limitation on input), background noise, buzzing, and even stochastic fluctuations were used as test vectors. The main purpose of test vectors selection was to examine most of vocoder's internal state and to build proper fixed point C-model, and then translate it on assembler for TMS320C54x.

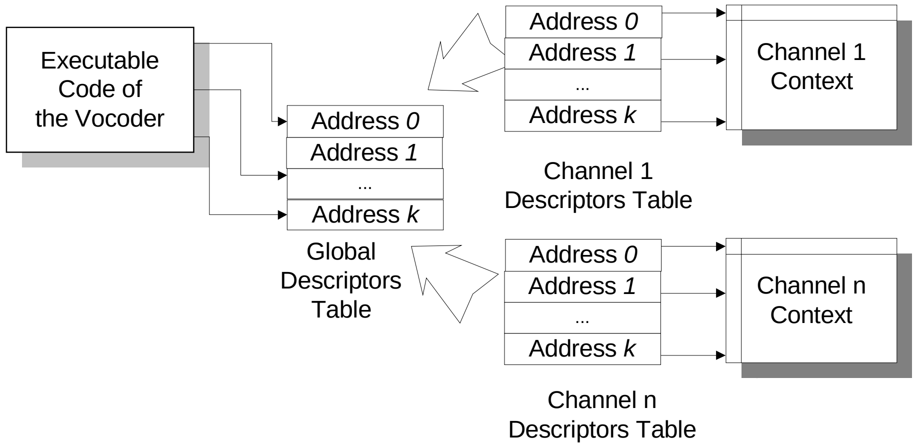

Fig. 4.

7. DTMF and Signaling Detection

Telephone line state analysis block can be divided into 2 separate parts: signaling detection and DTMF detection.
Two signaling detection algorithms were examined.
First one is based on dominating frequency principle. In this method the meaning of dominating frequency in signal spectrum is estimated on the basis of zero crosses number. Then that value is tested to belong to given frequency interval. Logical block of the algorithm provides detection of following signals: "dial tone", "ringing tone", "busy/congestion" with strictly defined timing characteristics. So this method is not flexible, but can be used on most of public telephone lines and PBX.
Second one is based on Goertzel's method and contains flexible parameters assignment using file on host-computer. Signals are given with the help of patterns, where frequency value, tone and pause lengths, corresponding deviations, and minimum repeat counter are set. These patterns are generated automatically by special host program as the result of phone line (connected to the gateway) signals processing. So this algorithm provides flexibility and stable detection of single- and double-tone station signaling, but needs more computational resource.
Two different algorithms of DTMF signals detection were investigated. First one exploits modified Goertzel's method with moving window, second one – set of adaptive notch-filters and zero crosses count as it was suggested in [4]. The second method provides more accurate results in comparison with spectral ones. The logical block guarantees high accuracy and noise stability. Usage of 16-bit arithmetic instead of 8-bit [4] greatly simplified the algorithm and improved its robustness.
On the base of carried out analysis Goertzel's algorithm with patterns loading was chosen for implementation of signaling detection, and algorithm [4] for DTMF signals detection. Usage of notch-filters method significantly reduced processor's loading (Table 1).

8. Features of TMS320C54x Usage.

For effective exploitation of TMS320C54x resources the specific of its RAM usage and memory mapping need to be taken into consideration. External memory usage requires additional wait states. Internal memory differs on the type of access (DARAM/SARAM) which also affects on program execution speed. That's why the program stack is situated in DARAM area, the system "heap" (for temporary data storing) is mapped also in this part of memory. Program code is located in SARAM area. Vocoders' codebooks tables, message queues and channel contexts are stored in external memory.
During debugging a specific feature of TMS320C54x which wasn't mentioned in documentation was discovered. After accumulator's left shift for more than 8 bits (in sign extension mode – SXM=1 and overflow mode – OVM=1) negative overflow can be obtained instead of positive, and vice versa.

9. Table of DSP Resources Usage.

Different functional blocks implementation parameters are given in Table 1.

Table 1

Functional Block	DSP Loading (MIPS)	Program memory (Kword)	Data memory (Kword)
TCELP 4.6 kbps	27	7.7	4.7 + 9.2 (tables)
G.723.1 (Annex A) 5.3/6.3 kbps	20/24	8.7	2.0 + 9.2 (tables)
G.729 (Annexes A and B) 8 kbps	13.34	9.65	3.1 + 3.0 (tables)
Echo Canceller 16 ms	4.6	0.7	0.7
AGC	0.4	0.05	0.01
A-law (G.711)	0.42	0.06	-
DTMF Signals Detector (Goertzel)	1.5	1.3	2.3
DTMF Signals Detector (Notch)	1.37	0.49	0.18
Station Signaling Detector	0.5	0.5	0.01
Real-time OS Kernel	5	3.8	0.8 (without buffers)

10. DSP Units Application Area

Developed DSP units can be used in wide area of IP and computer telephony devices.
In present time we use them in 2-, 8- and 16-channel IP-telephony gateways to provide point-to-point connection based on original handshake protocol for several groups of subscribers. Sample is shown on fig. 5. 2-channel DSP unit allows direct connection of telephone set omitting PBX.

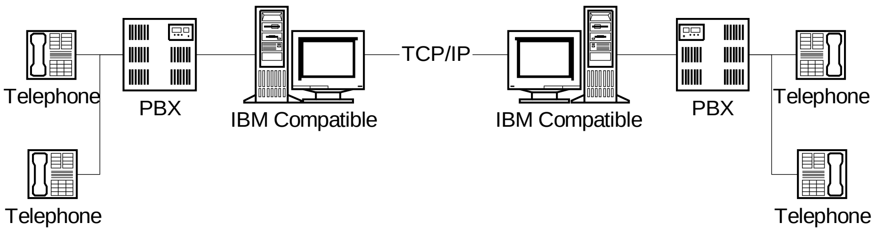

Fig. 5.

Besides that, 16-channel DSP unit together with two analog interface boards is used in information gathering and storage digital system. The system is implemented on a single PC working under FREE BSD operating system, and is designed for automatic continuous work with record/storage cycle of 45 days.
DSP units can be applied in multichannel voice-mail gateways, automatic telephone referral services, and answering machines.

11. Acknowledgments

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12. References

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